

interconnections to contact regions **35**, **41**, **53** (depending on how the device is being coupled to other circuit elements) and conventional passivation layers (not shown) above surface **23**, device **20** is substantially complete.

[0036] For transistors **20-1**, **20-2**, and **20-3**, the majority of carriers (e.g., electrons) are injected from first emitter region **40** into first base region **50** in an approximately vertical direction, which gives rise to a high current gain. In transistor **20-4**, most electrons are injected from emitter contact region **41-4** into lightly doped base region **263**, which can provide an even higher current gain than that attained in transistors **20-1**, **20-2**, **20-3**. The Early voltage of transistors **20-1**, **20-2**, and **20-3** is determined by two bipolar transistors connected in parallel. One bipolar transistor is formed by first emitter **40**, first base **50** and EPI **28**, and collector **30** at lateral distance **32-1**. Another bipolar transistor is formed by second emitter **43-1**, second base **51-1** in transistor **20-1**, second base **51-2** and EPI **28** between region **51-2** in transistor **20-2** and **20-3**, and BL collector **30**. For transistor **20-4**, portion **41-4** also plays an important role in determining the Early Voltage. When BL collector **30** is placed at least partially underlying emitter **43-1**, as for example in FIG. 1, high gain but relatively low Early Voltage are obtained. When BL collector **30** is pulled laterally away from emitter **43-1**, as for example in FIGS. 2-4, the current gain is reduced due to the larger base width but the Early Voltage is increased. Accordingly, BL collector **30** of bipolar transistors **20-1**, **20-2**, **20-3**, **20-4**, etc., can be placed in various lateral positions relative to first and second emitter regions **40**, **43**, thereby permitting a wide range of device characteristics to be obtained to suit specific applications, merely by mask changes without adding further process steps. In transistors **20-1**, **20-2**, **20-3**, **20-4**, emitter **43** has a moderate doping concentration, and it can be depleted by extrinsic base WELL **52** proximate junction **49** and by intrinsic base **51** underneath emitter region **43**, which significantly improves BV_{ceo}. A field plate located on STI region **55-11** above junction **49** (e.g., as shown for device **20-3** of FIG. 3) may be used to assist the depletion and further improve the break-down voltage. In addition, because of the relatively light doping of BL collector **30**, it can be fully depleted from all directions by the surrounding P-regions biased with the base (or other) potential when the collector voltage is high relative to other terminals. This combination of features significantly improves BV_{ceo} and BV_{cb0} and provides transistors **20-1**, **20-2**, **20-3**, **20-4** in FIGS. 1-5 a high side capability. Accordingly, transistors **20-1**, **20-2**, **20-3**, **20-4** facilitate tuning the bipolar transistor characteristics by, among other things, varying the position of the BL collector **30** relative to other elements without sacrificing the breakdown voltages and high side capability. This is very useful.

[0037] According to a first embodiment, there is provided a bipolar transistor (**20**), comprising, a semiconductor substrate (**29**) having a first surface (**23**), a first emitter region (**40**) of a first conductivity type in the semiconductor substrate (**29**) having a first emitter region doping concentration, a first base region (**50**) of a second, opposite, conductivity type in the semiconductor substrate (**29**) underlying the first emitter region (**40**, **41-4**) and having a first base region doping concentration, the first base region (**50**) forming a first PN or NP junction (**45**, **59**) with the first emitter region (**40**) at a first depth (**46**) from the first surface (**23**), a second emitter region (**43**) of the first conductivity type in the semiconductor substrate (**29**) having a second emitter region doping concentration and Ohmically coupled to the first emitter region (**40**), a

second base region (**51**) of the second conductivity type in the semiconductor substrate (**29**) underlying the second emitter region (**43**) and having a second base region doping concentration different than the first base doping concentration, the second base region (**51**) forming a second PN or NP junction (**47**) with the second emitter region (**51**) at a second depth (**48**) from the first surface (**23**), and a buried layer collector region (**30**) of the first conductivity type in the substrate (**29**) underlying the first surface (**23**) and laterally spaced a third distance (**32**) from the first emitter region (**40**). According to a further embodiment, the first emitter region (**40**) and the second emitter region (**43**) are laterally adjacent. According to a further embodiment, the first base region (**50**) and the second base region (**51**) are laterally adjacent. According to a still further embodiment, the first depth is greater than the second depth. According to a yet further embodiment, the second emitter region (**43**) lies laterally at least partly between the first emitter region (**40**) and the buried layer collector region (**30**). According to a still yet further embodiment, the second base region (**51**) lies laterally at least partly between the first base region (**50**) and the buried layer collector region (**30**). According to a yet still further embodiment, the transistor (**20**) further comprises a third emitter region (**41-4**) of a third emitter doping concentration and a third base region (**263**) of a third base doping concentration, wherein the third emitter region (**41-4**) is coupled to the first emitter region (**40**) and the third base region is coupled to the first base region (**50**) and the third base doping concentration is less than the first base doping concentration. According to another embodiment, the second emitter region (**43**) has a lateral extent (**44**) greater than the third distance (**32**). According to still another embodiment, the second emitter region (**43**) has a lateral extent (**44**) less than the third distance (**32**).

[0038] According to a second embodiment, there is provided a method for forming a bipolar transistor, comprising, providing a semiconductor containing substrate (**29**) with an upper surface (**23**), and having therein a buried layer collector region (**30**) of a first conductivity type located below the upper surface (**23**) and of a buried layer collector region doping concentration, wherein a first portion (**25**) of the substrate located below the buried layer collector region (**30**) and a second portion (**26**) of the substrate located above the buried layer collector region (**30**) are of a second, opposite, conductivity type, forming during one or more first doping steps in the second portion (**26**) of the substrate (**29**), first (**40**) and second (**43**) adjacent emitter regions of the first conductivity type near the first surface, the first emitter region extending substantially to the first surface and laterally separated from the buried layer collector region (**30**), and forming during one or more second doping steps in the second portion (**26**) of the substrate (**29**), first (**50**) and second (**51**) adjacent base regions of the second conductivity type, respectively, beneath the first (**40**) and second (**43**) emitter regions, wherein the first base region (**50**) has a first base region doping concentration and the second base region (**51**) has a second base region doping concentration different than the first base region doping concentration, and the first emitter region (**40**) and first base region (**50**) providing a first NP or PN junction (**45**) at a first depth (**46**) beneath the upper surface (**23**) and the second emitter region (**43**) and the second base region (**51**) providing a second NP or PN junction (**47**) at a second depth (**48**) beneath the upper surface (**23**). According to a further embodiment, the method further comprises providing at least one isolation region (**55-11**, **55-21**) substantially at the upper